LOW VOLTAGE PULL-DOWN CIRCUIT

Abstract of the Invention

A low voltage pull-down circuit for maintaining a node at a logic LOW voltage is provided. When a logic LOW is desired, the circuit provides a low-impedance path from the node to ground. The node may be easily pulled-up to a logic HIGH voltage, for example, by simply removing the low-impedance path and allowing a voltage source to reach the node through a resistor or transistor.

One embodiment includes the low voltage pull-down circuit in a power supervision circuit for systems that operate with, for example, low power conditions. The open-drain node is utilized as a power-on-reset node that provides a LOW logic signal to a system when the power being supplied to the system is below a pre-determined voltage threshold.